ABSTRACT

A hybrid summing module is presented, wherein the summing module comprises a hyperpipelined series of multiple full-adders, half-adders, and registers. The summing module may be implemented as a Wallace tree or as a Dadda tree. The structure of the adder tree is determined by maximally partitioning bits of equal significance into groups of three to serve as inputs to full-adders. Remaining groups of two are inputs to half-adders, while remaining single bits are passed directly to registers. In one embodiment each reduction stage serves as a pipeline stage. In another embodiment the summing module is used to sum the partial products of a multiplication operation with an additional input from an accumulator in the case of multiply accumulate operations. In yet another embodiment, the summing module accelerates complex multiply operations by feeding partial products from both terms resulting in real or imaginary components into the adder tree simultaneously.